Volume 07 Issue 02 Published, May 21, 2003 ISSN 1535-864X

Intel® Technology Journal

Intel® Centrino™ Mobile Technology

Mobile PC Platforms Enabled with Intel® Centrino™ Mobile Technology

A compiled version of all papers from this issue of the Intel Technology Journal can be found at:
http://developer.intel.com/technology/itj/index.htm

Mobile PC Platforms Enabled with Intel® Centrino™ Mobile Technology

Gordon Chinn, Mobile Platforms Group, Intel Corporation
Sanjiv Desai, Mobile Platforms Group, Intel Corporation
Eric DiStefano, Mobile Platforms Group, Intel Corporation
Krishnan Ravichandran, Mobile Platforms Group, Intel Corporation
Shreekant (Ticky) Thakkar, Mobile Platforms Group, Intel Corporation

Index words: Bluetooth™, Intel® Centrino™ mobile technology, Intel® WCS, WLAN, battery, coexistence, electronic cooling, notebook, power, validation, wireless

ABSTRACT

Mobile PC platforms enabled with Intel® Centrino™ mobile technology incorporate innovative technologies to significantly increase the mobility of notebook PCs. In this paper, we describe the following innovations:

- How to reduce interference between wireless communication technologies using the Intel® Wireless Coexistence System (Intel® WCS).
- Two techniques for significantly extending average platform battery life.
- Simple thermal solutions for thinner and lighter form factors.

Finally, we outline a comprehensive platform-level validation process that helps deliver a stable platform with Intel quality.

INTRODUCTION

Platforms enabled with Intel Centrino mobile technology incorporate innovative technologies to significantly increase the mobility of notebook PCs. This paper describes innovations in reducing interference between wireless communication technologies, extending average platform battery life, and in driving a thermal solution for thinner and lighter form factors.

When multiple wireless technologies such as Bluetooth* Wireless LAN, and Wireless WAN are embedded in the same mobile system, the risk of interference between these radio frequency (RF) technologies greatly increases because of their close proximity to each other. In this paper we discuss general technical RF challenges for mobile platforms and describe innovative techniques used on platforms enabled with Intel Centrino mobile technology. These techniques mitigate interference by using the Intel Wireless Coexistence System (Intel WCS).

We also discuss new and advanced platform power-management features for improved battery life. Two new techniques are described: asynchronous voltage regulator (VR) control with a power status indicator (PSI), and multiphase Intel® Mobile Voltage Positioning (IMVP).

Platforms enabled with Intel Centrino mobile technology also incorporate state-of-the-art techniques to enable compact, lightweight thermal solutions in smaller form factor systems. The design includes an efficient remote heat exchanger, an air flow set aside for system cooling, and system venting, that together cool the processor and the system as a whole, using only a single fan. The latest interface materials, heat pipe technology, and fans provide the required performance in a small package.

Finally, Intel validation best-known methods (BKMs) are applied to ensure that these platforms deliver optimum

---

® Intel and Intel Centrino are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

* Other names and brands are the property of their respective owners

® Intel is a trademark of Intel Corporation or its subsidiaries in the United States and other countries.

system performance with multiple wireless technologies operating concurrently within the enterprise as well as when connected to hotspots outside the enterprise.

WIRELESS TECHNOLOGIES

Platforms enabled with Intel Centrino mobile technology incorporate innovative radio frequency (RF) technologies to significantly increase the mobility of notebook PCs. These technologies include Wireless Personal Area Networking (WPAN), e.g., Bluetooth; Wireless Local Area Networking (WLAN), e.g., 802.11a and 802.11b; and Wireless Wide Area Networking (WWAN), e.g., General Radio Packet Service (GPRS). Integrating multiple wireless technologies greatly enhances connectivity to the enterprise Intranet and the Internet, as well as to peripherals such as PDAs, printers, and headsets.

Radio Frequency Challenges in Mobile Notebook PCs

When incorporating RF technologies into a digital computing environment such as a notebook PC, traditional system designers are faced with new challenges previously relegated to RF engineers. Antennas must be added for each frequency band. Since notebook PCs generally consist of many metallic components such as framing structures, hard drives, displays, antenna radiation patterns can be greatly distorted. This distortion can potentially cause significant RF performance variations, as the notebook PC's physical orientation is varied relative to the location of the intended communicating device such as an access point (AP), a peripheral such as a printer, and even another notebook PC.

These RF technologies consist of very sensitive receivers and potentially high-power transmitters. When multiple RF technologies are embedded (co-existent) in the same notebook PC, the risk of interference between these technologies is greatly increased as the transmitters of one radio can couple with the sensitive receivers of another radio, even if they operate in different frequency bands. Technologies such as Bluetooth and 802.11b have even greater interference risks since they both operate in the same 2.4GHz frequency band. Antenna isolation techniques mitigate some of these interference issues, but with multiple antennas and decreasing form factor sizes, optimal placement of antennas is not always possible. New interference-mitigating technologies are then required. For example, Intel Centrino mobile technology includes the Intel Wireless Coexistence System (Intel WCS), which significantly mitigates the interference between 802.11b and Bluetooth technologies.

Intel Wireless Coexistence System

While antenna isolation provides some interference mitigation between 802.11b and Bluetooth radios, performance is still impacted to some degree. For example, 802.11b data throughput is degraded by Bluetooth interference, even with 40dB of antenna isolation, as shown by the lower curve in Figure 1. The upper curve shows the ideal throughput when no Bluetooth interference is present.

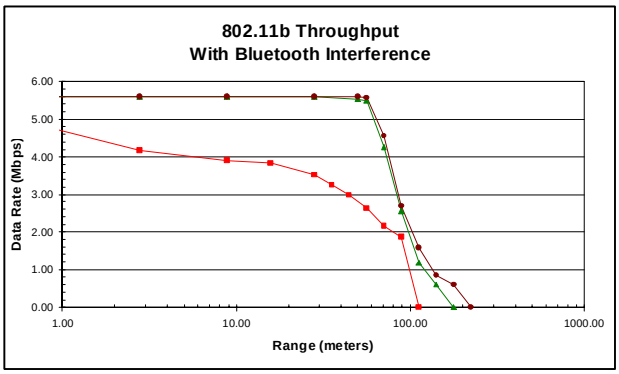

Figure 1: 802.11b throughput with Bluetooth interference

To further mitigate interference between Bluetooth and 802.11b, Intel WCS was developed as one of the Intel Centrino-enabling technologies. Intel WCS consists of a combination of antenna isolation techniques, a channel exchange (Figure 2), and priority signaling between an Intel PRO/Wireless Network Connection 802.11 solution and a third-party Bluetooth module. Phase 1 of Intel WCS has been implemented: it mitigates Bluetooth interference and restores 802.11b data throughput nearly completely as shown by the chart in Figure 1.

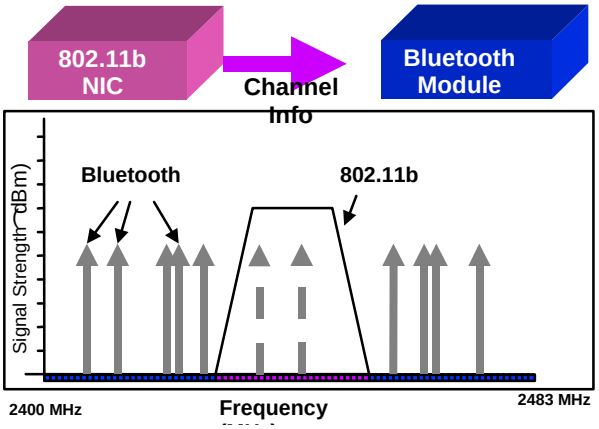

Figure 2: Intel WCS Channel Exchange

Intel WCS is designed to complement the Adaptive Frequency Hopping (AFH) interference mitigation algorithm being developed by the Bluetooth Special Interest Group (SIG). AFH will mitigate the impact of

802.11b on Bluetooth data throughput, but only between AFH-compliant Bluetooth devices as shown in Figure 3.

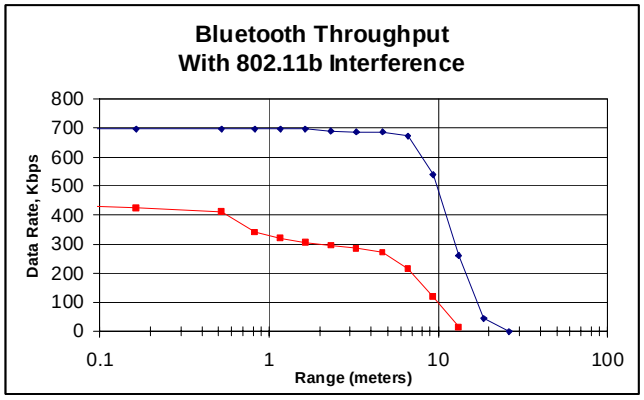

Figure 3: Bluetooth throughput with 802.11b interference

Phase 2 of Intel WCS will add Bluetooth priority signaling from the Bluetooth module to the Intel PRO/Wireless network connection, resulting in a restoration of connection reliability for both AFH and non-AFH (legacy) Bluetooth devices as shown in Figure 4.

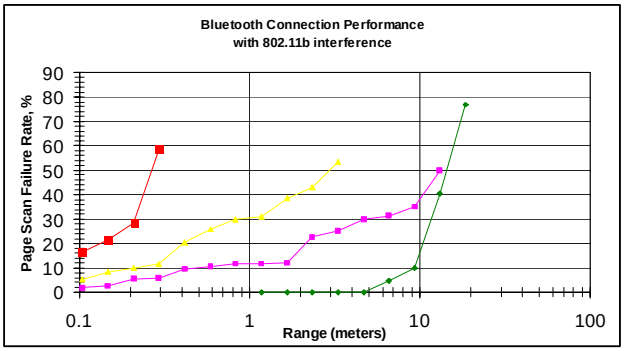

Figure 4: Bluetooth connection performance

Bluetooth Enabling

Multiple third-party Bluetooth silicon and module vendors have been enabled to be compatible with Intel WCS, including SiliconWave and Cambridge Silicon Radio. Extensive verification and validation testing has been completed with these silicon vendors, providing pre-validated system solutions to the customer.

In summary, integrating multiple RF technologies into mobile notebook PCs provides new challenges to systems designers, including antenna gain uniformity and interference mitigation. Intel WCS, an Intel Centrino mobile technology, provides powerful interference mitigation between 802.11b and Bluetooth and enhances AFH.

EXTENDED BATTERY LIFE TECHNIQUES

The battery life of a mobile PC is a function of the power consumed by each of its components and the capacity of the battery. Figure 5 shows the breakdown of the power consumption of a typical notebook while running the battery life benchmark Ziff-Davis BL4.01.

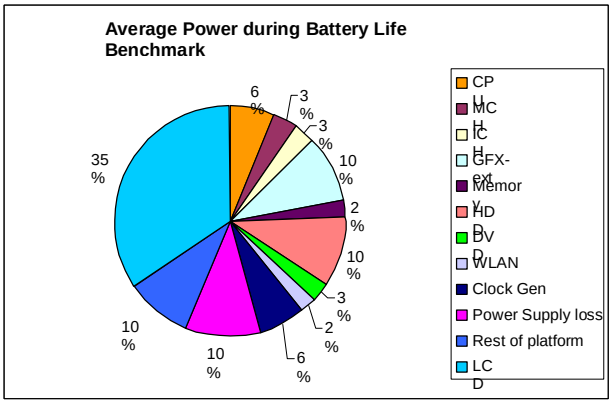

Figure 5: Platform average power distribution

As can be seen, some of the largest power consumers are the display (LCD), power supply, hard disk drive (HDD) and graphics. It is also noteworthy that the CPU is one of the lowest consumers of battery life power (only consumes 6%) due to the advanced power-management built into the processor (Intel SpeedStep® technology, QuickStart, Deep Sleep, etc.) To learn more about processor power management, please see "Intel® Pentium® M Processor Power Estimation, Budgeting, Optimization, and Validation" in this issue of the *Intel Technology Journal*.

On Intel Centrino mobile technology, Intel developed and enabled the following *techniques* to reduce the power consumption of some of these subsystems and to help increase the battery life:

- Asynchronous Voltage Regulator (VR) Control with Power Status Indicator #
- Multiphase Intel Mobile Voltage Positioning (IMVP) technology

Asynchronous Voltage Regulator Control with PSI#

The fully power-optimized CPU represents a very complicated load to the voltage regulator (VR). This is because its current draw can range from a few mAs to several tens of Amperes, depending on the workload put on the processor. The transitions from low to high currents can also occur rapidly (in ms). This makes it difficult for the VR designer to maintain high-power

conversion efficiency in the full operating range. Typically, the efficiency is maximized at the highest end of the current range. However, the power-conversion efficiency of the VR drops off quickly toward the low-power condition. This is because the standby or quiescent (zero output loading) power of the VR is approximately 0.2-0.5W, which is comparable to the low-power CPU load, causing the efficiency to be <50%.

In a battery life benchmark, such as the ZDBL4.01, the processor spends >80% of the time in the low-current state (C3). Therefore, it is very important to maximize the power-conversion efficiency of the VR during the C3 state to extend the battery life of the notebook. The Asynchronous VR control with PSI# is a method used to increase the efficiency of the VR during the C3 state, without affecting the efficiency during the high-power state.

A VR is used to convert an unregulated high input voltage, either the AC/DC adapter or battery, to a suitable regulated DC voltage rail to power the core of the CPU. In this particular application, the regulated voltage is 1.35V ± 7.5%, including VR DC error, noise, and transient response error, etc. A switching voltage regulator is used to produce high-power conversion efficiency. Due to the high current demand of the CPU, this VR operates in a continuous synchronous topology.

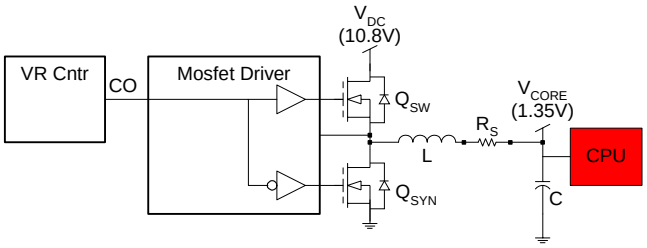

Figure 6: Synchronous VR

Referring to Figure 6, a VR is used to regulate the battery voltage (8.1-12.6V, 10.8V nominally) down to 1.35V for the CPU core rail. A VR controller monitors the output voltage, V_{CORE}, and compares it to an internal 1.35V reference.

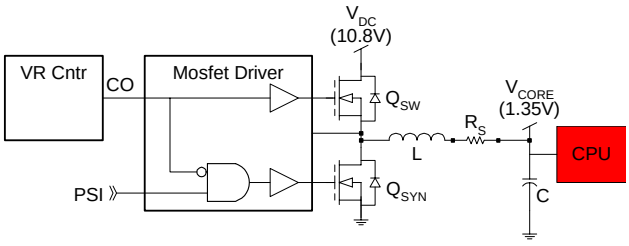

Figure 7: Non-synchronous VR with CPU power status indicator

Referring to Figure 7, the logic driving the gate of Q_{SYN} is gated, in addition to CO, by a Power Status Indicator (PSI). PSI, when LO, keeps the gate of Q_{SYN} low regardless of CO level. When PSI is HI, the Mosfet driver drives the gate of Q_{SYN} normally. In this application, the STP_CPU# signal can be used in place of a PSI.

The Geyserville-III transition (Performance Optimized Mode to Battery Optimized Mode) also requires additional modifications due to the voltage differences between the two modes. Figure 8 shows the final circuitry that is used in Intel Centrino mobile technology.

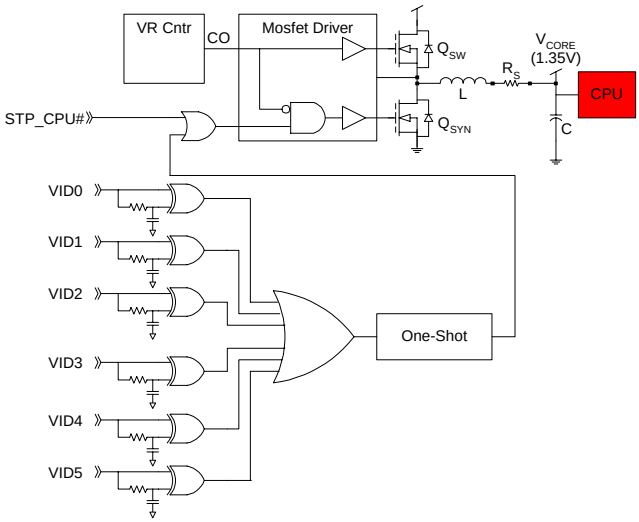

Figure 8: STP_CPU# override with VID code

Optimized Intel Mobile Voltage Positioning

A CPU enabled with Intel SpeedStep technology operates at a different CPU core frequency. For example, when operating with an AC adapter plugged into the notebook, battery life is not an issue, as power is always available (although power consumption can limit performance as the internal temperature may rise.) The CPU is placed into a Performance-Optimized Mode (POM), where the core frequency is high (i.e., 1GHz). When operating from the battery as the input power source, the CPU is placed into the Battery-Optimized Mode (BOM) where the core frequency is dropped to a lower value (i.e., 600MHz) to reduce power consumption. The CPU power demand for POM is higher than that of BOM. More importantly, the current demand for POM is much higher than for BOM. This means the output-decoupling requirement for POM is much worse than that for BOM. The CPU voltage tolerance is ± 7.5% for both POM and BOM because the Intel Mobile Voltage Positioning (IMVP) load line remains constant for both POM and BOM. Therefore, when switched to BOM, using the GMUXSEL signal

(with low indicating that the CPU is in BOM and high indicating POM), the output voltage can be "shifted" down to reduce power consumption.

Intel Mobile Voltage Positioning Design Implementation

Figure 9 shows positive offset voltage is controlled by $R_{OFFSET-P}$. A small-signal mosfet switch is added in series with this resistor and ground. During POM, GMUXSEL is high connecting $R_{OFFSET-P}$ to ground, providing a positive offset voltage. During BOM, GMUXSEL is low turning off the mosfet, removing the positive offset voltage.

During DeepSleep state, a negative offset voltage is applied through $R_{OFFSET-N}$ and pulled down with the STP_CPU# signal.

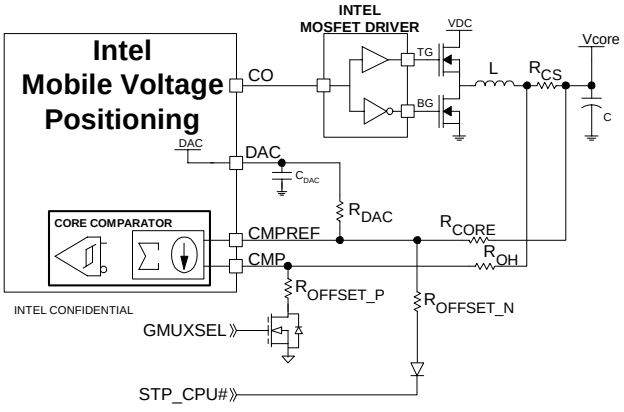

Figure 9: IMVP implementation

RESULTS

The techniques were implemented on two IBM T20 notebooks with 600 MHz Pentium® III processors. All data, unless mentioned otherwise, are averaged power numbers measured during the entire battery discharge (~3-4 hours duration) during a Ziff-Davis Battery Life benchmark, ZDBL4.01.

To establish accurate improvement (if any), a baseline measurement is first established. Two complete ZDBL runs were performed on a new T20 notebook platform with the same battery pack charged overnight each time. An average runtime was calculated along with an average platform/battery power measurement.

® Pentium III is a registered trademark of Intel Corporation or its subsidiaries in the United States and other countries.

CPU Intel Mobile Voltage Positioning Feature Results

Figure 10 shows a battery from a charged status, 12.0V, down to a discharged status, ~8.5V. The average power over the entire ZDBL run of 3 hours, 40 minutes is 11.77W.

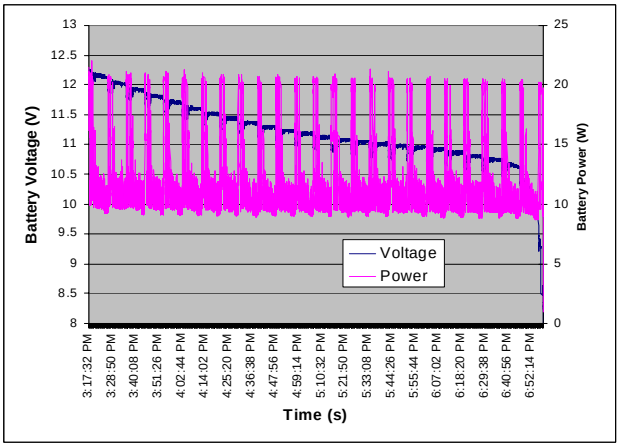

Figure 10: Discharge battery voltage/power profile–baseline

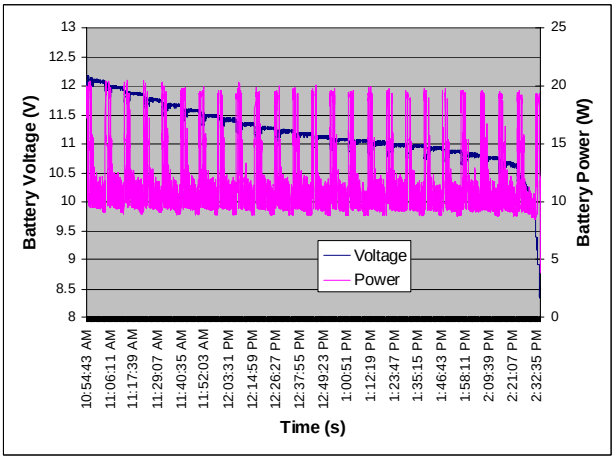

Figure 11: Discharge battery power profile with CPU IMVP VR

Measurements after CPU Intel Mobile Voltage Positioning Modification show the average power over the entire ZDBL run is 11.49W. This is a 280mW power reduction in the CPU during the ZDBL run (see Figure 11).

Non-Synchronous Voltage Regulator with PSI# Results

Figure 12 shows the battery discharge power over the entire 3 hour, 15 minute ZDBL run of the IBM T20 notebook used for this study.

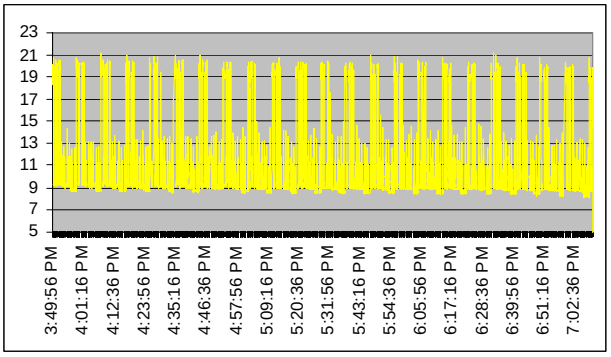

Figure 12: Discharge battery power profile–baseline

The average power over the entire ZDBL run of 3 hours, 19 minutes, is 10.94W.

With the non-synchronous VR with PSI# (STP_CPU#) implemented, the discharge profile is as shown in Figure 13:

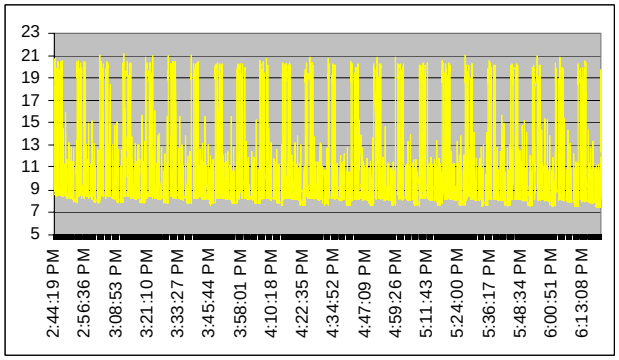

Figure 13: Discharge battery power profile with STP_CPU# VR

The average power over the entire ZDBL run of 3 hours, 36 minutes, is 10.36W. This is a 580mW power reduction in the CPU VR.

In summary, as demonstrated in the above experiments, the two features implemented on the IBM T20 can result in over 1W of power savings during the battery life benchmark (ZDBL4.01) run. While the benefits may vary with different OEM systems, the expectation is that these will save power and improve the life of the battery.

THERMAL DESIGN

The Intel Centrino mobile technology platform can be cooled using a simple, compact, light-weight solution. The approach, though simple, is fundamentally important to successful design. In this section, we discuss a strawman set of requirements, the overall cooling approach, cooling performance expectations, and the resulting cooling solution design.

For the purposes of this discussion, we define a set of strawman requirements comprising the system form-factor, a platform power scenario, and a set of boundary conditions. We assume a system thickness of 25 mm (total base and display) with a footprint of 320x260 mm, which accommodates a 15" display. This thin form-factor allows for approximately a 13 mm inside height below the keyboard, for a solution design. We further assume a power scenario in which the processor may be at 24.5W, and all the other components may be at 18.5W, for a total of 43W in the base of the system (see Figure 14).

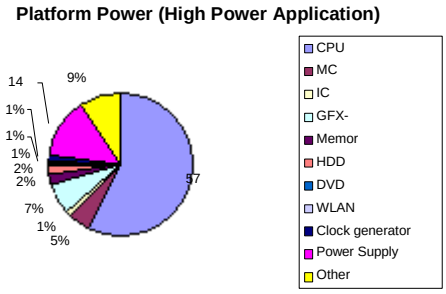

Figure 14: Platform TDP power

Finally, important boundary conditions are the maximum temperature difference allowed between the component and the user ambient $\Delta T_{j\text{-}a}$. For the CPU, we assume 65ºC. Additionally, any given system design must consider chassis surface temperatures as well as acoustic limits on fan noise, for ergonomic constraints.

The overall thermal solution approach is illustrated in Figure 15:

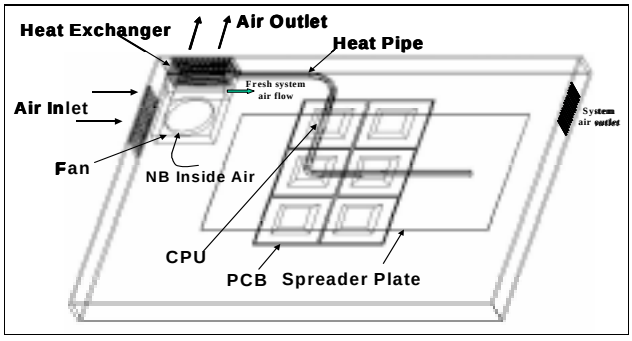

Figure 15: Notebook layout illustration

It includes the now conventional remote heat exchanger approach for component cooling, but with fresh air flow capability set aside to provide cool air to the system. The fresh air flow is important to cool components and especially to keep skin temperatures cool. The passive cooling limit (i.e., dissipation by radiation and natural convection from the base of the system) is approximately 18W, allowing for a chassis skin temperature of roughly 15ºC above ambient as is observed in typical system designs; close to the non-processor power assumed above.

The overall cooling performance expectations are identified using the equation below:

$$\theta_{j-a} = \frac{\Delta T_{j-a} - T_{system}}{P_{CPU}}$$

where P_{CPU} is the power we need to cool and ΔT_{j-a} is as discussed above. T_{system} represents the net impact of the power of the rest of the platform on the component, in this case the processor and the thermal solution. The value of T_{system} is dependent upon system design and is best approximated prior to design by using system simulations. Assuming 10ºC for the strawman scenario discussed above, the required performance θ_{j-a} is 2.25°C/W.

Figure 16 illustrates schematically the remote heat exchanger cooling solution and important locations of temperatures. The overall performance θ_{j-a} is further approximated by the equation below:

$$\theta_{j-a} \approx \theta_{j-hp} + \theta_{hp-a}$$

where θ_{j-hp} is the thermal resistance from the component junction to the heat pipe and θ_{hp-a} is the remaining resistance from the heat pipe to the ambient temperature through the heat exchanger. θ_{j-hp} includes resistance of conduction through silicon, the interface material and contact resistances, and the resistance of the evaporator (region over the heat source) of the heat pipe. With new thermal interface materials, suitable thermal attach and heat pipe design, a performance of approximately 0.45 C-cm2/W can be achieved on a reference die. For performance verification, direct communication with respective suppliers is recommended. All components of θ_{j-hp} are affected by the source they are cooling and are considered in θ_{j-hp}. Although the Intel® Pentium® M processor uses 0.13 micron process technology, the design is optimized to mitigate the effects of a smaller source, and the effective θ_{j-hp} translates to approximately 0.9ºC/W.

Prototypes from fan and heat exchange suppliers indicate that 1.1ºC/W can be achieved for θ_{hp-a}. However, the θ_{hp-a} value must be de-rated to allow for fresh air to be set aside for system cooling. Although the passive limits are close to those accommodated by the maximum passive limits, spreading is not perfect, and an allowance must be made for system constraints on effective passive dissipation. We assume 15% θ_{hp-a} performance set aside to complement system cooling. It is important to note that the air flow is provided directly from the exhaust of the fan and flows underneath the motherboard to best protect skin temperature. Two very important features of the system design provide short and direct air flow paths into the fan and out of the heat exchanger and adequate system air outlet vents, respectively.

Figure 16 shows a design rendition of the solution. The weight and volume of prototypes are approximately 55g and 4.3cm^3, respectively, approximately one-third the weight and size of solutions for higher-power processors.

In summary, the thermal solution for Intel Centrino mobile technology platforms is compact and lightweight, utilizing only a single fan to cool the processor and the system.

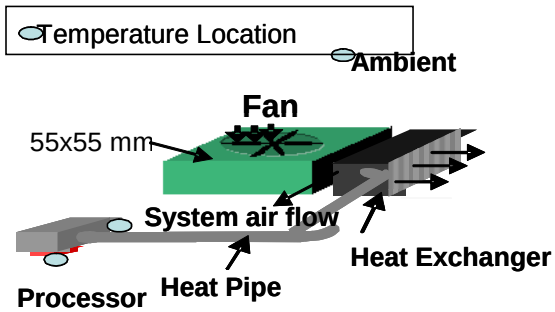

Figure 16: Thermal solution

PLATFORM-LEVEL VALIDATION

This section outlines the comprehensive platform-level validation process that helped deliver a stable platform with Intel quality. Intel validation BKMs were applied to ensure that a mobile platform with Intel Centrino mobile technology delivered optimum system performance with multiple wireless technologies operating concurrently within the enterprise as well as when connected to hotspots outside the enterprise.

The goal for the platform with Intel Centrino mobile technology was extended validation of all platform components to maximize reliability and interoperability.

® Pentium M is a registered trademark of Intel Corporation or its subsidiaries in the United States and other countries.

This validation was primarily divided into the following three categories (see Figure 17):

1. Validation of Intel and Third-Party Vendor (TPV) Intel Centrino mobile technology-enabled platform components.
2. Validation of Intel Centrino mobile technology-enabled platforms on customer reference boards.
3. End-User system validation.

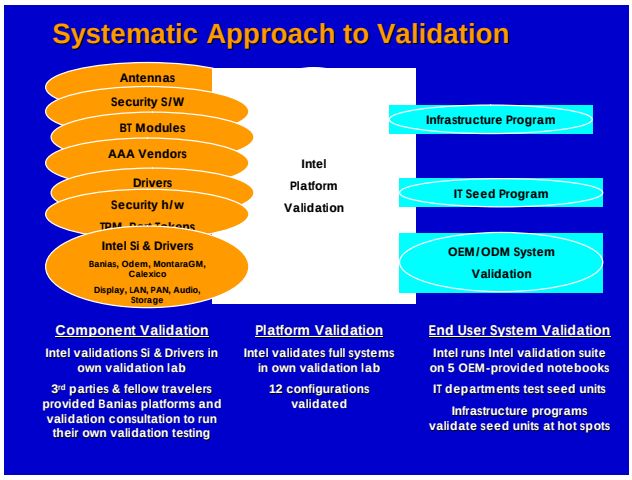

Figure 17: Systematic approach to validation

Figure 18 shows Intel and TPV delivered components on a platform with Intel Centrino mobile technology. Each Intel component underwent thorough comprehensive system and compatibility validation using Intel validation BKMs traditionally used on processors and chipsets. To ensure high-quality validation of TPV components, Intel worked with TPVs to define comprehensive test plans for validation of their components using Intel validation BKMs.

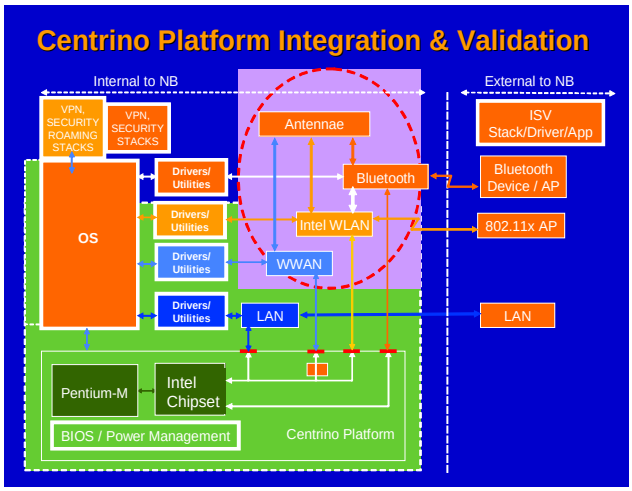

Figure 18: Intel Centrino technology platform integration and validation

The focus of platform-level validation was the integration of Intel Centrino mobile technology components on an Intel Customer Reference Board platform and the performance of comprehensive compatibility and interoperability validation under mobile-specific stress test conditions as well as under typical usage-model scenarios. Figure 19 shows some examples of platform validation tests.

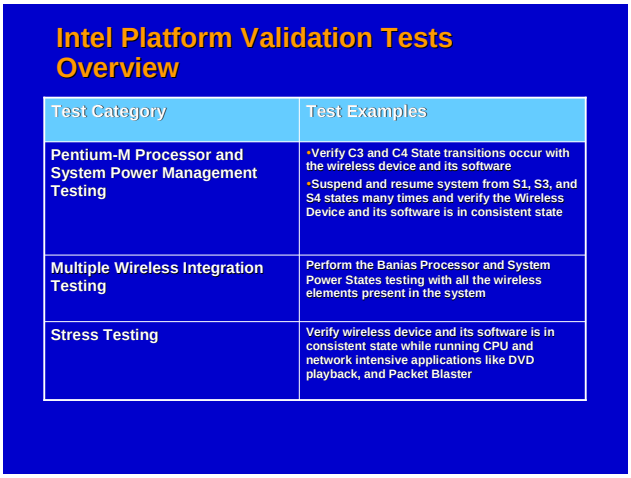

Figure 19: Platform validation test examples

The third type of validation was platform-level validation using Intel Centrino mobile technology-based OEM systems. The focus was testing in a real end-user environment. For example, multiple Intel Centrino mobile technology-based systems with multiple platform configurations were tested for compatibility with industry- standard Wireless LAN (WLAN) access points at various hotspots.

Intel Wireless Verification Program

As part of establishing Intel Centrino mobile technology as the premier Wireless LAN notebook PC client, Intel worked with many leading companies to accelerate the deployment of 802.11 wireless communication capabilities in private and public spaces. The overall goal is to help reduce the two major Wi-Fi adoption barriers: availability and awareness. The program works with traditional and emerging Wi-Fi providers and key location owners to achieve the following:

1. Deploy Wi-Fi in locations relevant to the business traveler, such as airports, hotels, and franchise chains.
2. Verify Intel Centrino mobile technology in the installed infrastructure.

3. Raise the awareness of the availability of the service in these locations by directed co-marketing programs and a signage program.

CONCLUSION

Platforms enabled with Intel Centrino mobile technology incorporate innovative technologies to significantly increase the mobility of notebook PCs. We described the following innovations:

- Details are given on how to reduce interference between wireless communication technologies. The Intel Wireless Coexistence System is demonstrated to basically recover all WLAN performance under Bluetooth interference.
- Two new, advanced platform power-management features for improved battery life are described in this paper: Asynchronous VR control with PSI, and multiphase IMVP. These features implemented on an IBM T20 can result in over 1W of power savings during the battery life benchmark (ZDBL4.01) run. While the benefits may vary with different OEM systems, the expectation is that these will save power and improve battery life
- By coupling state-of-the-art thermal techniques with the advanced platform power-management features for lower power consumption, the thermal solution for a typical platform with Intel Centrino mobile technology was demonstrated to be compact and lightweight, utilizing only a single fan to cool the processor and the system.

Finally, the Intel Centrino mobile technology platform is extensively tested and tuned for components of Intel Centrino mobile technology to optimally work together in order to maximize reliability and interoperability and to deliver on all four mobility vectors. Intel Centrino mobile technology continues to undergo extensive security validation with industry-standard security and leading third-party security solutions. Intel is continuing to conduct comprehensive infrastructure verification with the wireless LAN infrastructure ecosystem and public wireless LAN service providers.

ACKNOWLEDGMENTS

The authors thank the following individuals for their contributions: Al Bettner for antenna development and enabling; Marlon Cardenas and Je-Young Chang for driving thermal solution development; Camille Chen for driving WLAN coexistence integration and validation; Randy Durrant for Intel WCS systems design and Bluetooth enabling; Eddie Lin for driving Bluetooth coexistence integration and validation; Don Nguyen for developing the detailed white papers on each of these initiatives, which provided much of the data that is incorporated into this paper; and Francis Truntzer for co-developing and driving wireless platform validation strategy.

REFERENCES

For more information on Extended Battery Life Program, please access the following Web site:
http://developer.intel.com/design/mobile/battery.htm

AUTHORS' BIOGRAPHIES

Gordon Chinn is the Radio Frequency (RF) Systems Architecture manager in Intel's Mobile Platforms Group (MPG) and is responsible for enabling mobile platform PCs with multiple, concurrent, embedded radio technologies. He has over 30 years of experience in various RF communications development positions in the commercial and aerospace industry. Gordon holds a B.S. and M.S. degree in Electrical Engineering and Computer Science from the University of California at Berkeley. His e-mail is gordon.chinn@intel.com.

Sanjiv Desai is the Mobile Systems and Wireless Architecture manager in Intel's Mobile Platforms Group (MPG). He is responsible for the definition and architecture of mobile platforms at Intel. He has over 20 years of industry experience in various CPU, Chipset, and System design and development positions at Intel, National Semiconductor, and American Microsystems Inc. (Gould). Sanjiv holds an M.Sc. degree in Electrical Engineering from North Carolina A&T State University (USA) and a B.Sc. degree in Electrical Engineering from M.S. University (India). His e-mail address is sanjiv.c.desai@intel.com.

Eric DiStefano is the manager of the Thermal Tools and Technology team in the Mobile Platforms Group. He has been with Intel defining thermal solutions for mobile processors and platforms for five years. Prior to Intel, he worked in the aerospace industry for 15 years developing advanced space propulsion, propellant feed systems, and cooling of various systems including avionics. His e-mail is eric.distefano@intel.com.

Krishnan Ravichandran has a B.S.E.E. degree from IIT Madras, India and an M.S.E.E. degree from Carnegie Mellon University. He joined Intel in 1988 after completing his M.S. degree and has spent his entire career in the Mobile Group, performing a variety of roles (circuit design, chipset lead, CPU Design Manager, Program Manager, Platform Architecture and more recently Extended Battery Life Manager). His e-mail is krishnan.ravichandran@intel.com.

Shreekant (Ticky) Thakkar is the co-director of Mobile Platform Architecture in Intel's Mobile Platforms Group (MPG). He has over 24 years of experience in various development and planning positions at Intel and Sequent (now part of IBM). Ticky established direction for mobile notebook PCs to transition from portable to wireless computing–making the notebooks deliver the best wireless Internet experience. Ticky holds Ph.D. and M.S. degrees in Computer Science/Engineering from the University of Manchester (England) and a B.S. degree in Computer Science/Statistics from the University of Manchester. His e-mail is ticky.thakkar@intel.com.

For further information visit:

developer.intel.com/technology/itj/index.htm